Abstract

A circuit for regulating a sensed current in a power transistor is provided. The circuit is configured to sense if the drain current of the power transistor has reached a limit current I_{limit}. A sense transistor is arranged in an m:1 current mirror relationship with the power transistor. Additionally, a current sink that is coupled to the drain of the sense current is also configured to sink a current approximately equal to I_{limit}/m. Further, a comparison circuit is configured to compare the drain voltages of the power and sense transistors. Also, if the drain current of the power transistor is less than I_{limit}, a current sink pulls down the drain of the sense transistor, so that the drain voltage of the sense transistor is less than the drain voltage of the power transistor. However, if the level of the drain current of the power transistor reaches I_{limit}, then Vds of the sense transistor would reach Vds of the power transistor, and the comparator would trip. Additionally, two switches are arranged to be open when switching currents flowing through the power transistor and sense transistors are each substantially zero. By opening the switches when these switching currents are each substantially zero, a false output (trip) of the comparison circuit can be prevented.